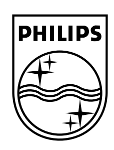
DATA SHEET

TDA2615
2 × 6 W hi-fi audio power amplifier

Product specification
Supersedes data of July 1994
File under Integrated Circuits, IC01

1995 May 08

Philips Semiconductors



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FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with *“IEC 268”* and *“DIN 45500”*
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2615 is a dual power amplifier in a 9-lead plastic single-in-line (SIL9MPF) medium power package. It has been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	V_S = ±12 V; THD = 0.5%	–	6	–	W
G_v	internal voltage gain		–	30	–	dB
$\|G_v\|$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA2615	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1

BLOCK DIAGRAM

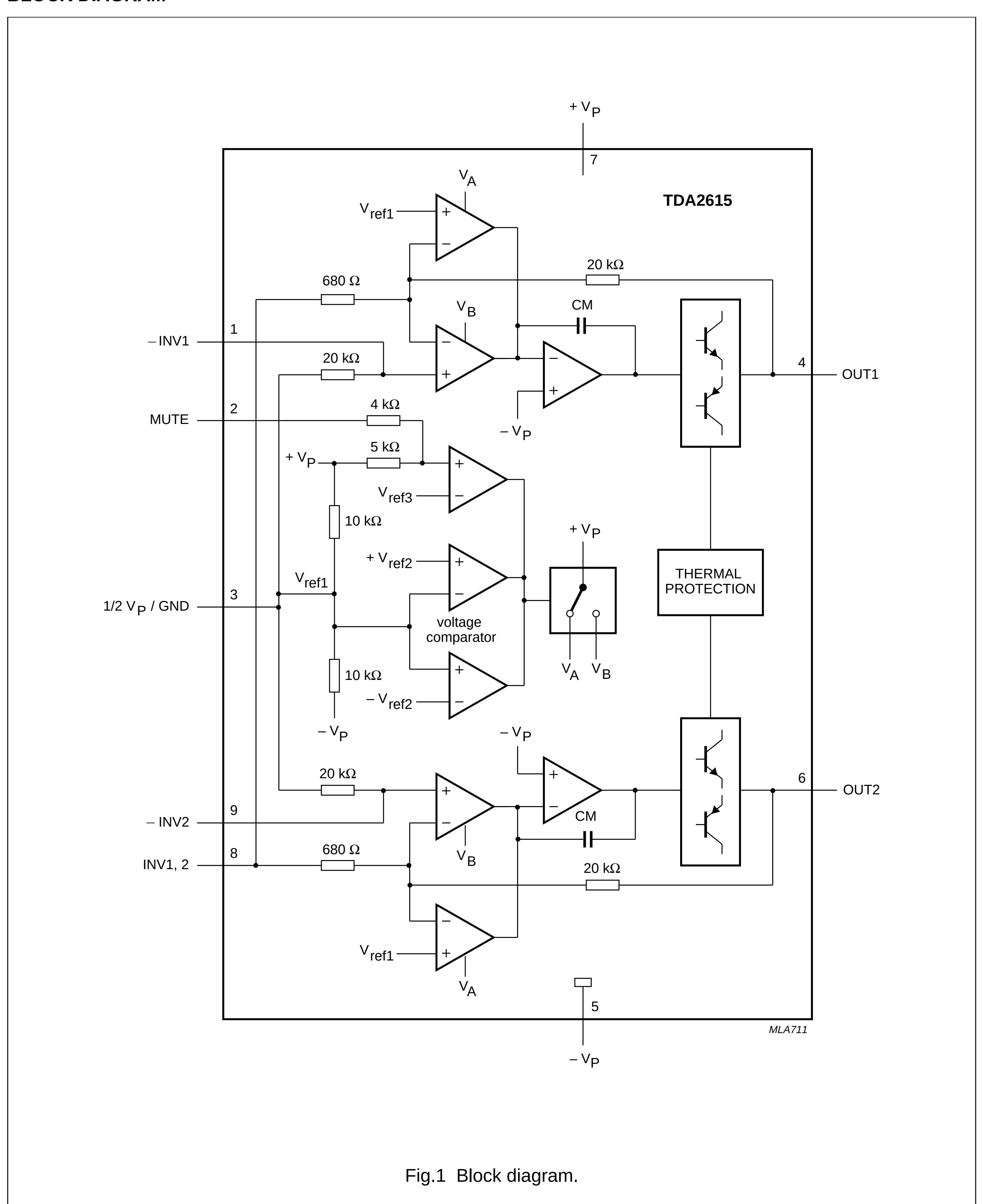


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
½V_P/GND	3	½ supply voltage or ground
OUT1	4	output 1
–V_P	5	supply voltage (negative)
OUT2	6	output 2
+V_P	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
–INV2	9	non-inverting input 2

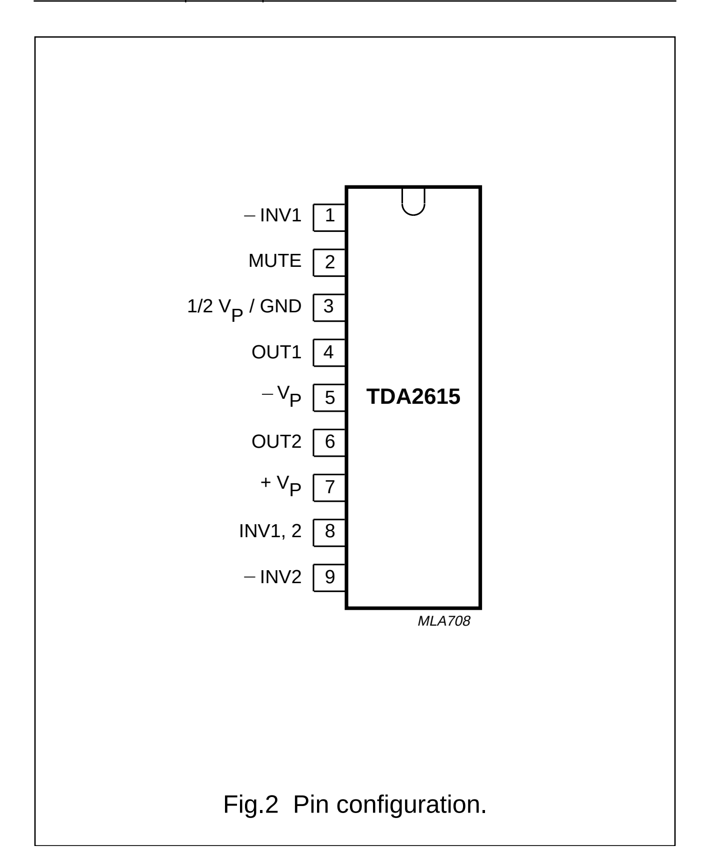


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2615 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and stereo TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 × 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±12 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 µA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 6 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_S = ±12 V, the measured maximum dissipation is 7.8 W.

With a maximum ambient temperature of +60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{7.8} - 6 = 5.5 \text{ K/W}$$

The metal tab has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	15	W
T_{stg}	storage temperature range		–55	+150	°C
T_{xtal}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	+150	°C
t_{sc}	short-circuit time	short-circuit to ground; note 1	–	1	h

Note

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V **(with the load short-circuited)**. For symmetrical power supplies the circuit is short-circuit-proof up to V_P = 21 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	6	K/W

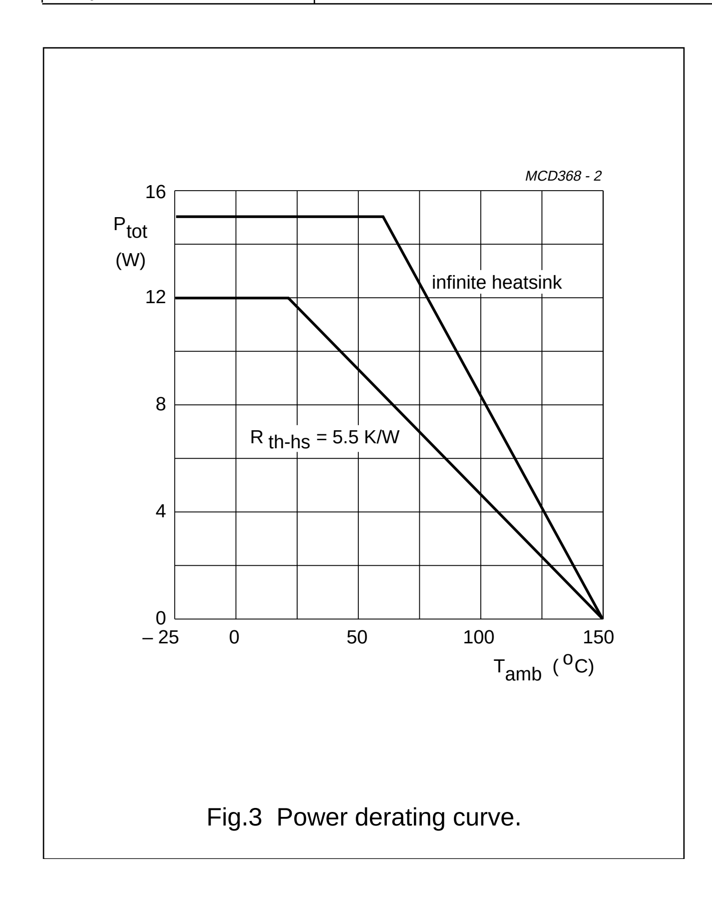


Fig.3 Power derating curve.

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	12	21	V
I_{ORM}	repetitive peak output current		2.2	–	–	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	12	21	V
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power	THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α_{cs}	channel separation	$R_S = 0$	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating position; note 6						
$I_{q(tot)}$	total quiescent current		18	40	70	mA
P_O	output power	THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 1	–	40 to 20000	–	Hz
G_v	voltage gain		29	30	31	dB
$\|G_v\|$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\|Z_i\|$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α_{cs}	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
$I_{q(tot)}$	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\|\Delta V_{off}\|$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA

Notes

1. $V_P = \pm12$ V; $R_L = 8$ Ω; $T_{amb} = 25$ °C; $f_i = 1$ kHz; symmetrical power supply $I_{MUTE} = < 30$ μA (see Fig.4).
2. The power bandwidth is measured at a maximum output power (P_{Omax}) of –3 dB.
3. The noise output voltage (RMS value) is measured at $R_S = 2$ kΩ, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at $R_S = 0$ and $f_i = 100$ Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at $f_i = 1$ kHz.
5. $\pm V_P = 4$ V; $R_L = 8$ Ω; $T_{amb} = 25$ °C; $f_i = 1$ kHz; symmetrical power supply (see Fig.4).
6. $V_P = 24$ V; $R_L = 8$ Ω; $T_{amb} = 25$ °C; $f_i = 1$ kHz; asymmetrical power supply $I_{MUTE} < 30$ μA (see Fig.5).
7. The internal network at pin 2 is a resistor divider of typical 4 kΩ and 5 kΩ to the positive supply rail. At the connection of the 4 kΩ and 5 kΩ resistor a zener diode of typical 6.6 V is also connected to the positive supply rail. The spread of the zener voltage is 6.1 to 7.1 V.

TEST AND APPLICATION INFORMATION

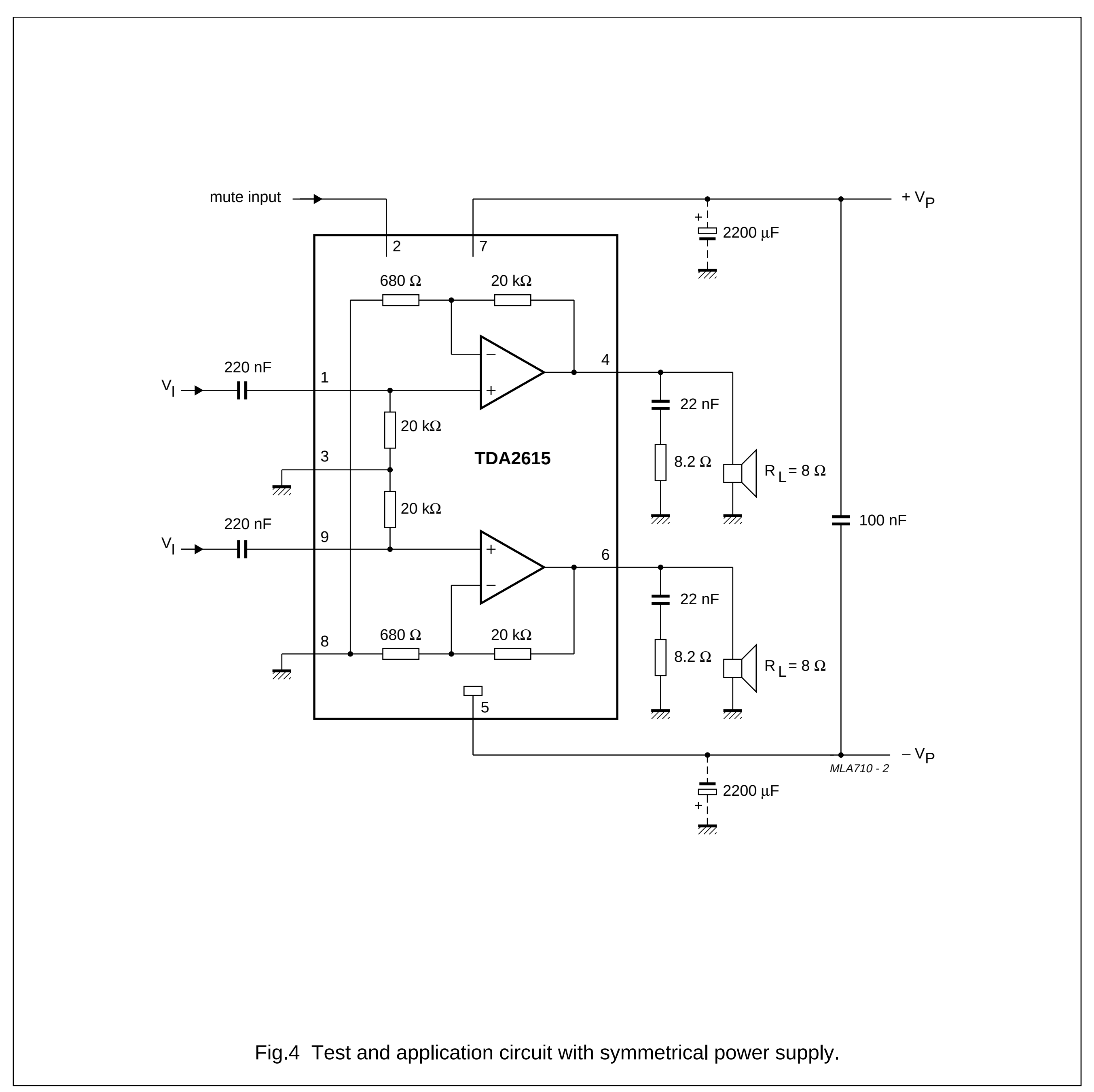


Fig.4 Test and application circuit with symmetrical power supply.

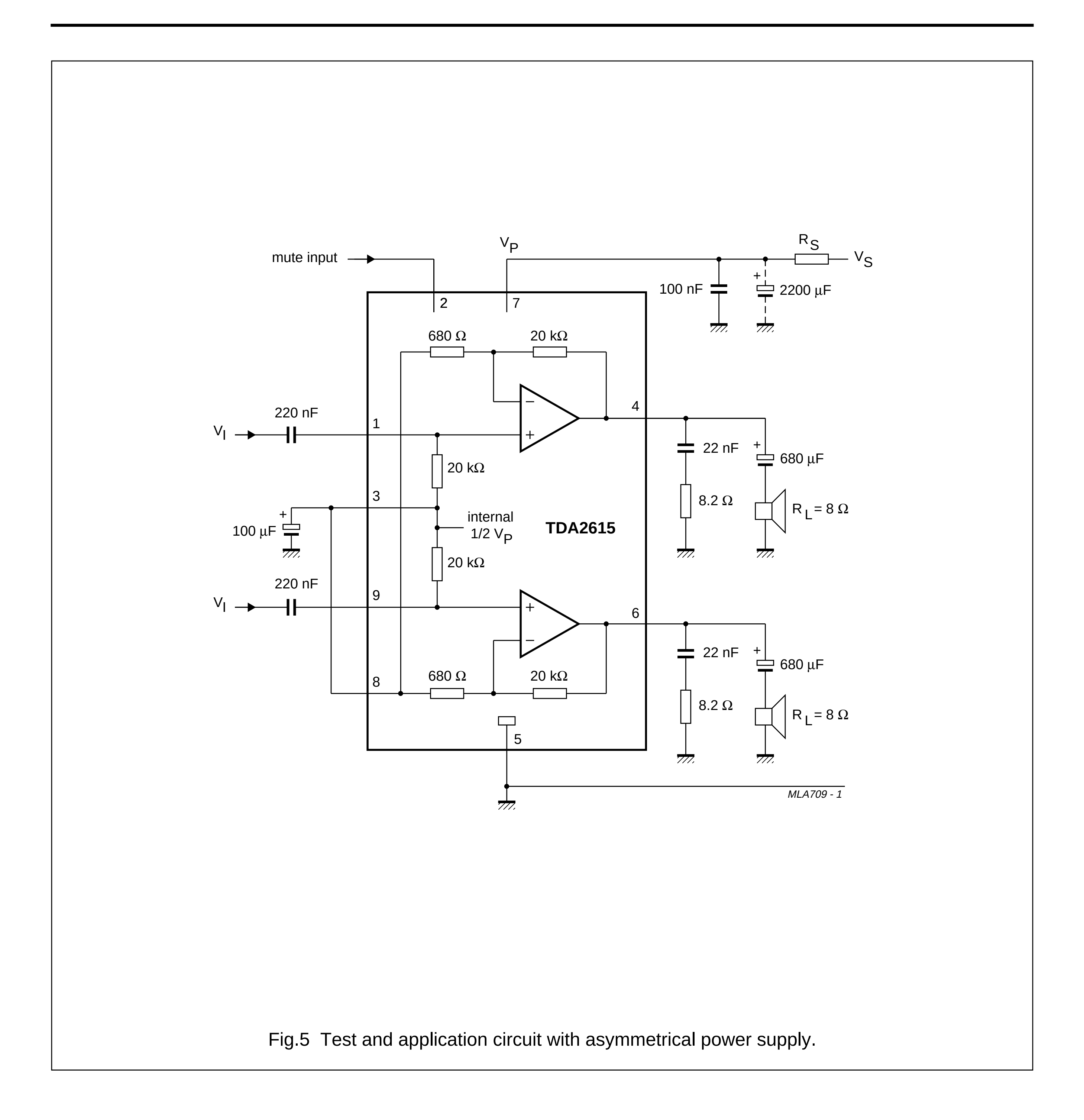
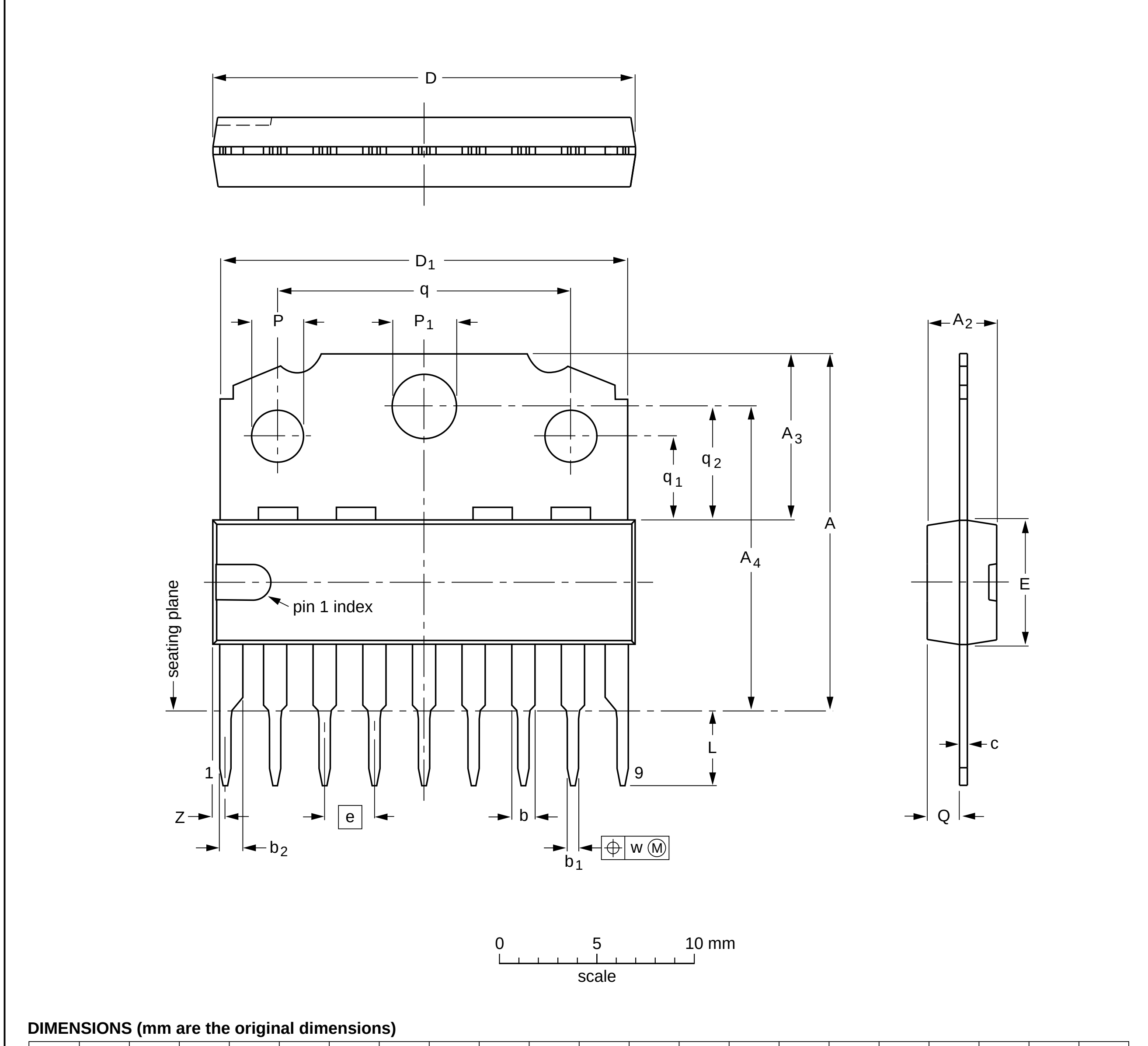


Fig.5 Test and application circuit with asymmetrical power supply.

PACKAGE OUTLINE

SIL9MPF: plastic single in-line medium power package with fin; 9 leads **SOT110-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	D(1)	D_1	E(1)	e	L	P	P_1	Q	q	q_1	q_2	w	Z(1) max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						~~92-11-17~~ 95-02-25

SOLDERING

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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